EE/CprE/SE 491 WEEKLY REPORT 04

3/1/2020 – 3/15/2020

Group number: 08

Project title: High Resolution Digitally Trimmable Resistor

Client &/Advisor: Prof. Randy Geiger

Team Members/Role: Clark Reimers - Test Engineer, Pierce Nablo - Design Engineer, Alek Benson - Information Manager, Oluwatosin Oyenekan - Meeting Lead

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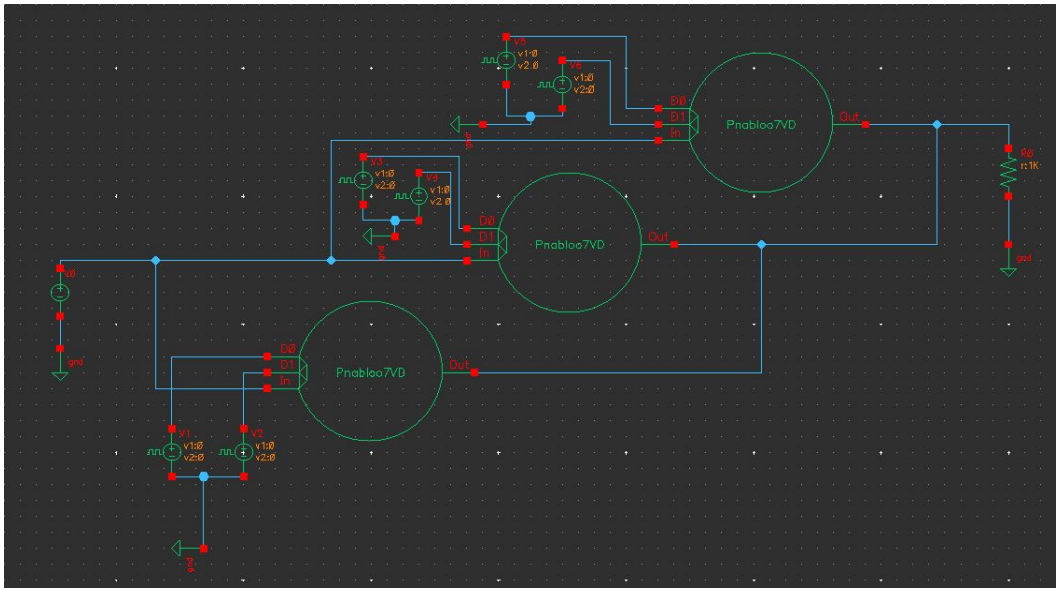
❖ Weekly Summary

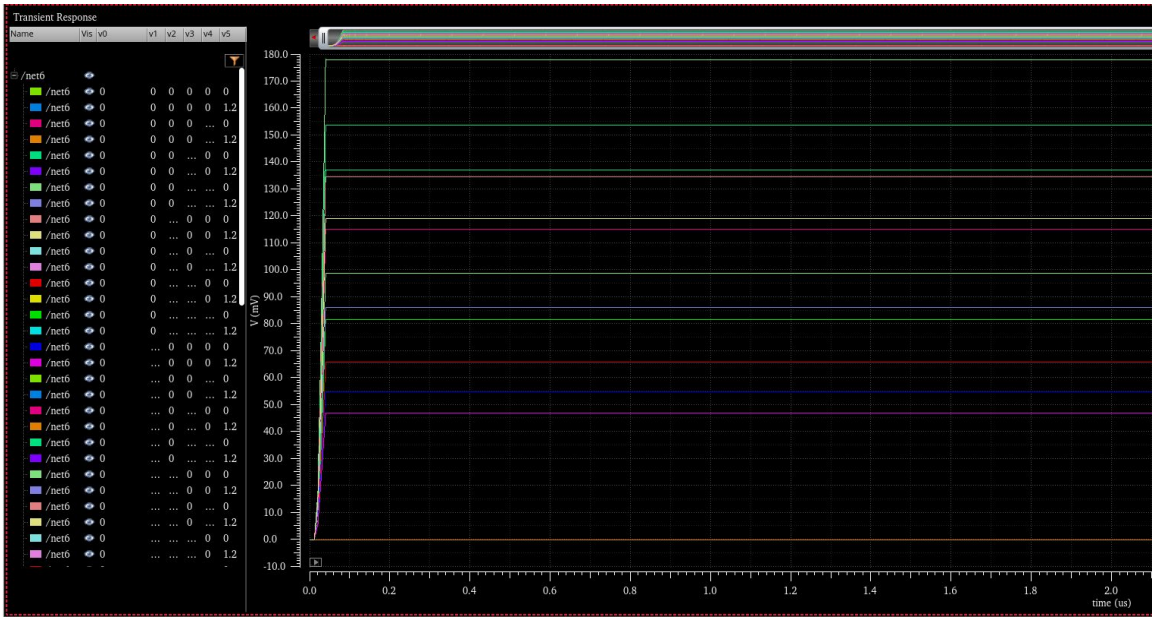
During the past 2 weeks, the group created many potential designs in Virtuoso. The two test designs were simulated and compiled into documented results. New potential designs were created in Virtuoso and symbols were created to simplify future, more complicated designs. We simulated these designs to analyze the behavior of the circuit. Varying the input voltages, gate voltages, and operating temperatures allowed us to discover the output characteristics. Designs and Simulations were evaluated and presented in the weekly meetings with Dr. Geiger.

❖ Past week accomplishments

Clark Reimers:

- Assisted in schematic simulations
    - Started simulations of one of our designs

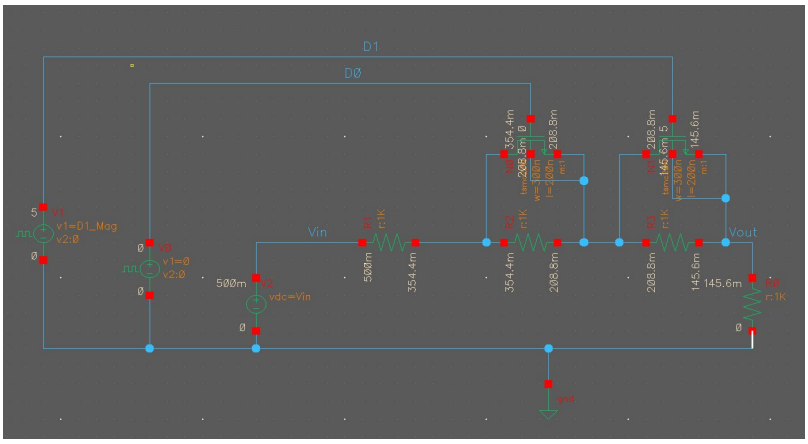


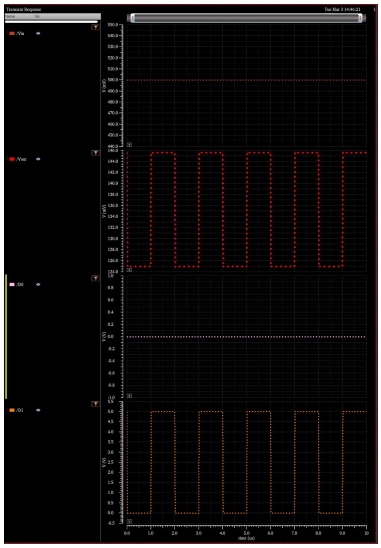


- Presented current findings to professor Geiger and the team to discuss relevance of results and get feedback
- Lightning talk
- Started working on finding the temperature coefficient
- Assisted in completion of regular weekly assignments for senior design

Pierce Nablo:

- Simulated schematics for a couple designs in virtuoso.

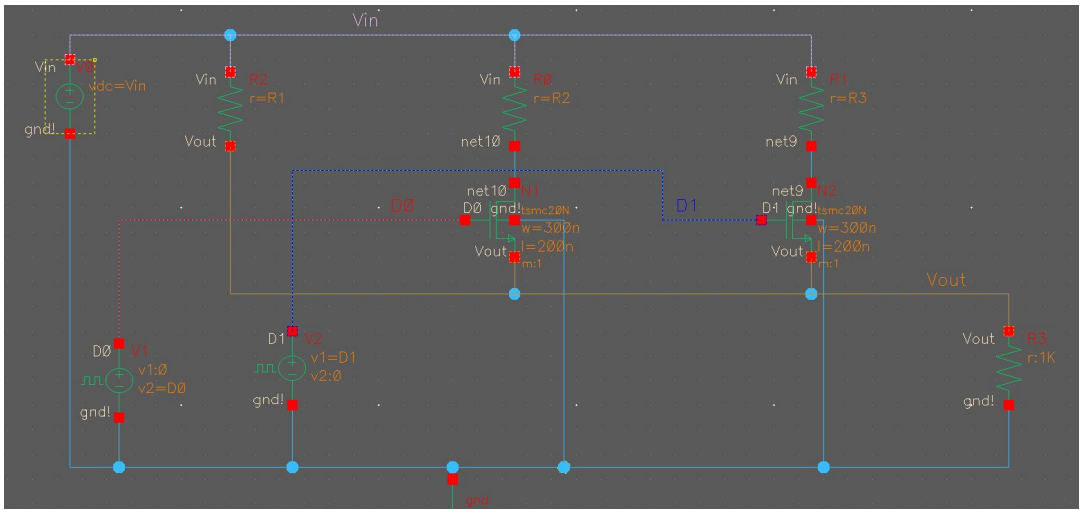




- Presented to Dr. Geiger the simulation results
- Edited the Lightning talk
- Completed weekly assignments for EE491

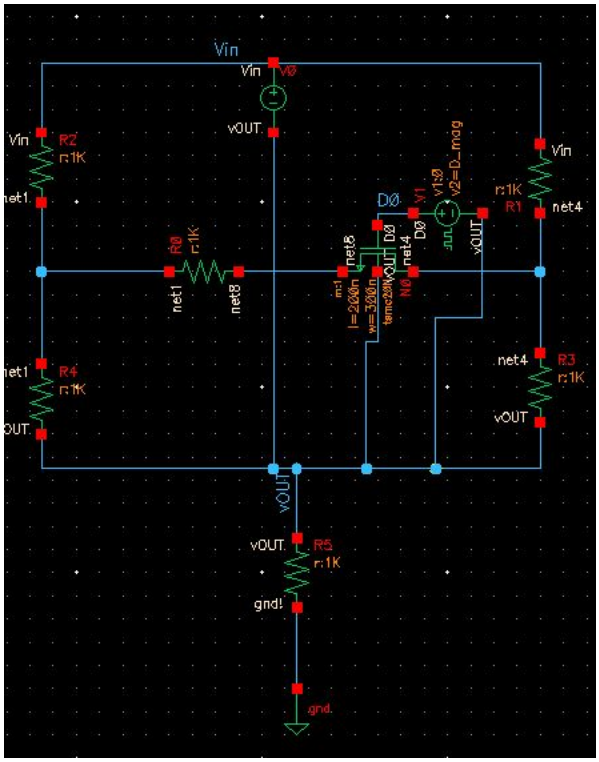
Alek Benson:

- Continued learning 330/435 material.
- Continued researching negative temperature coefficient options.
- Worked on setting up a Virtuoso environment on my linux machine profile.

- Worked on organizing our team work folder on Google Drive for our extra design schematics and simulation results.
- Worked on the design of the ladder structure as a potential design structure.
- Worked on the sweeping the temperature parameter to get our initial TC for nmos.
- 

Oluwatosin Oyenekan:

- Simulated the ladder structure design on virtuoso
- Presented to Dr Geiger and the team my findings
- Organized our weekly meetings.
- Completed weekly assignments for EE491



❖ **Pending issues**

Clark Reimers:

- We need to make sure that the team is ready to move to remote work for at least the next three weeks.

Pierce Nablo:

- No issues

Alek Benson:

- No issues

Oluwatosin Oyenekan:

- No Issues

❖ **Individual contributions**

Name	Hours this period	Hours cumulative
Clark Reimers	11	50
Pierce Nablo	12	51
Alek Benson	12	47
Oluwatosin Oyenekan	12	48

❖ **Plans for the upcoming week**

Clark Reimers: Our group's collective goal is to get the temperature coefficients for the different circuits we have looked at so far; especially the reference circuits. I would like to work with my group to achieve this goal. I would also like to continue researching how to bypass the temperature dependency issue and continue improving on our existing structures. Finally, I would like to make some updates to our team website.

Alek Benson: The plan is to keep learning from Geiger's 330/435 slides. Also, plan to simulate all current designs using temperature variations and get TC results. Then, test adding some NTC circuit components and re-simulate.

Oluwatosin Oyenekan: The plan for this week is to begin designing and simulating the design ideas we came up with and present it to Gieger. My goal for this period is to test out and get a positive result from at least one circuit.

Pierce Nablo: For the next week I want to try and get the temperature coefficients for the series, parallel and array circuits that we made during this past week. In addition I want to expand the circuits we made this past week to have more bits of resolution.

- **Summary of weekly advisor meeting**

  The meeting was held in our weekly scheduled meeting room in Coover and was productive. Slides were shown to present findings from simulations of the test designs and our potential designs that were created. Non-ideal characteristics of the switches were identified and discussed, and the need for testing of temperature coefficient was discussed. A clear understanding of the project's current state and next steps was achieved. The second week in this period was not discussed with Dr. Geiger as he was planning to be out of town. We continued working on testing our initial schematics in the second week.